What is Claimed is:

1. In a target processor, apparatus for storing a events related to the generation of a trigger signal, the apparatus comprising:

a plurality of event signal generation units, each event signal generation unit providing an event signal in response to a preestablished target processor condition

a trigger generation unit coupled to the plurality of event signal generation units, the trigger generation unit responsive to at least one preselected event signal for generating an associated trigger signal, the trigger generating unit generating a trigger control signal; and

a register, the register having the event signals applied to the trigger unit applied thereto, the register responsive to a trigger control signal generated along with the trigger signal, the trigger control signal causing the register to store event signals applied thereto.

2. The apparatus as recited in claim 1 further comprising at least one event signal generating unit, each event signal generating unit generating an event signal upon identification of a predetermined condition in the target processor.

3. The apparatus as recited in claim 1 further comprising a read bus, wherein a second control signal

causes the contents of the register to be applied to the read bus.

4. The apparatus as recited in claim 3 wherein the register is a memory-mapped register.

5. The apparatus as recited in claim 1 further comprising:

a second register, the second register responsive to the control signal for storing a program counter address related to the conditions in the target processor resulting in the events signals.

6. The method of storing an events signals resulting in the generation of a trigger signal, the method comprising:

generating an event signal for each predetermined event;

applying each event signal to a trigger generation unit;

applying each event signal to a preselected storage unit location;

when a predetermined event signal or predetermined combination of event signals is applied to the trigger generation unit, the trigger generation unit providing a trigger signal and a trigger control signal; and

applying the trigger control signal to the storage unit, the storage unit storing the event signals in the storage unit in response to the trigger control signal.

7. The method as recited in claim 6 wherein the storage unit is a register.

8. The method as recited in claim 6 wherein applying a control signal to the storage unit results in application of the contents of the storage unit to a read bus.

9. The method as recited in claim 6 further comprising the step storing program counter address in a second storage unit in response to the trigger control signal.

10. A target processor comprising:

at least one event detection unit, each event detection unit responsive to predetermined condition of the target processing unit for generating a related event signal;

a trigger generation unit, the trigger generation unit generating trigger signal in response to at least one of the related event signals, the trigger unit generating a trigger control signal when the a trigger signal is generated; and

a storage unit, the storage unit coupled to the event detection unit, the storage unit storing each event

signal is a related storage unit location in response to the trigger control signal.

11. The target processor as recited in claim 10 further comprising a read bus coupled to the storage unit, the event signals stored in the storage unit being applied to the read bus in response to a second control signal.

12. The target processor as recited in claim 11 wherein the storage unit is a memory-mapped register accessible to an external test and debug device.

13. The target processor as recited in claim 10 further comprising a second storage unit, the second storage unit having a program counter address applied thereto, the storage unit storing applied program counter address in response to the trigger control signal.

14. The target processor as recited in claim 13 further comprising a delay line, the delay line delaying the application of the program counter address to the second storage unit for a predetermined period of time.

15. The target processor as recited in claim 14 wherein the second storage unit is a memory-mapped register.